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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,136	03/19/2004	Matthew F. Davis	8381/ETCH/SILICON/JB1	8916

55649 7590 06/01/2009

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EXAMINER	
ANGADI, MAKI A	

ART UNIT	PAPER NUMBER
1792	

NOTIFICATION DATE	DELIVERY MODE
06/01/2009	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MATTHEW F. DAVIS, LEI LIAN, and
BARBARA SCHMIDT

Appeal 2009-002782
Application 10/805,136
Technology Center 1700

Decided: [1]May 28, 2009

Before TERRY J. OWENS, JEFFREY T. SMITH, and
JEFFREY B. ROBERTSON, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

The Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1, 3-21 and 36-53. Claims 22-27, which are the only other pending claims, have been withdrawn from consideration by the Examiner. We have jurisdiction under 35 U.S.C. § 6(b).

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the Decided Date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

The Invention

The Appellants claim a method for controlling the fabrication of integrated circuit devices. Claim 1 is illustrative:

1. A method of controlling a process of fabricating integrated devices on a substrate, comprising:

measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on the substrate:

adjusting a process recipe of an etch process for etching the substrate and a process recipe of at least one post-etch process using the results of measuring the dimensions on the structures; and

executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure.

The References

Morgenstern	2003/0022510 A1	Jan. 30, 2003
Krivokapic	6,567,717 B2	May 20, 2003
Fairbairn	6,625,497 B2	Sep. 23, 2003
Choo	2004/0078108 A1	Apr. 22, 2004 (filed Oct. 21, 2002)
Perry	2004/0087041 A1	May 6, 2004 (filed Nov. 1, 2002)

The Rejections

The claims stand rejected under 35 U.S.C. § 103 as follows: claims 1-18 and 36-53 over Fairbairn in view of Choo, Krivokapic and Perry, and claims 19-21 over Fairbairn in view of Choo, Krivokapic, Perry and Morgenstern.

OPINION

We affirm the Examiner's rejections.

The Appellants argue only the independent claims, i.e., claims 1 and 36 (Br. 4-7; Reply Br. 4-8). Although an additional reference (Morgenstern) is applied to dependent claims 19-21, the Appellants do not provide a substantive argument as to the separate patentability of those claims (Br. 7; Reply Br. 8). We therefore limit our discussion to the independent claims. The dependent claims stand or fall with the independent claim from which they depend. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2007).

Issue

Have the Appellants shown reversible error in the Examiner's determination that the applied references would have rendered prima facie obvious, to one of ordinary skill in the art, a process comprising measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on a substrate, and executing a multi-pass process in which, while forming the at least one structure, the substrate is processed more than once by a measurement process, an etch process and at least one post-etch process?

Findings of Fact

Fairbairn reduces "CD [critical dimension] variation by feeding back information gathered during inspection of a wafer (e.g., after photoresist development) to upcoming lots that will be going through the photolithography process, and by feeding forward information to adjust the next process the inspected wafer will undergo (e.g., the etch process)" (col. 4, ll. 41-46). If measured parameters deviate from design dimensions, 1) information on photolithography stepper focus and exposure can be fed back to the photolithography photo cell so the stepper can be adjusted, either

automatically or at the user's discretion, to correct the deviation in following lots, and 2) an etch recipe to correct the error can be fed forward to the etcher and implemented automatically or at the user's discretion to process wafers in the inspected lot (col. 4, l. 63 – col. 5, l. 7).

Choo makes measurements during semiconductor fabrication that "can be utilized to generate feed forward and/or feedback control data that can [be] utilized to selectively adjust one or more fabrication components and/or operating parameters associated therewith to achieve desired results (e.g., critical dimensions within acceptable tolerances and/or mitigation of overlay)" (¶ 0005). The measurements "can be analyzed to generate feedback/feed forward information that can be utilized to adjust operating parameters of processing components to which the same or other die are/will be subjected to mitigate undesired results" (¶ 0042).

Krivokapic discloses a wafer etching method wherein "[n]onconforming, post-etch wafers may be thrown away if over-etched, or returned for further etching (rework) if under-etched" (col. 10, ll. 35-37).

Perry discloses "a method for detecting an endpoint in a recess etch process by monitoring the absolute recess depth that takes into account such factors as incoming material variations" (¶ 0008).

Analysis

The Appellants acknowledge that multi-pass processes were known in the art, and state that their invention is a method for controlling such a process (Spec. ¶¶ 0003, 0005).

The Appellants argue that Fairbairn, Choo and Perry do not disclose a multi-pass process (Br. 4-6; Reply Br. 4).

That argument is not well taken because the Examiner relies upon Krivokapic with respect to the Appellants' multi-pass process claim limitation (Ans. 6-7).

The Appellants argue (Reply Br. 5):

> [I]t is clear that *Krivokapic* merely recites that, after measurement, if the wafer is over-etched and unsalvageable, then the wafer may be thrown away, but if the wafer is under-etched and may be saved, then it may be returned for re-work. Such re-work is not a multi-pass process as defined in the claims.

"[D]uring examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification." *In re Translogic Tech. Inc.*, 504 F.3d 1249, 1256 (Fed. Cir. 2007), quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000).

The Appellants' Specification states, in the "Description of the Related Art" section, that "[f]abrication of the micro-electronic devices may comprise multi-pass processes in which one or more layers of a film stack of the device are repeatedly deposited and selectively etched, thereby forming structures of the devices being fabricated" (Spec. ¶ 0003).

Thus, the broadest reasonable interpretation of "multi-pass process" in view of the Appellants' Specification includes the conventional process in which multiple layers are deposited and etched to form a film stack. The Appellants' claims require measuring at least one pre-etch dimension and at least one post-etch dimension, and require a multi-pass process that includes a measurement process, an etch process and at least one post-etch process (and/or pre-etch process in claim 36). Those claim requirements would be met by applying Krivokapic's re-etch process to the layers of the

conventional stack or Fairbairn's etched layer, i.e., measuring an etched layer to determine whether the etching conforms to specifications (which corresponds to the Appellants measuring at least one pre-etch dimension), re-etching a layer that is under-etched (which corresponds to the Appellants' etch process), and repeating that sequence until the desired degree of etching is obtained (which corresponds to the Appellants' post-etch process). As stated in *KSR Int'l. Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) , "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." One of ordinary skill in the art, through no more than ordinary creativity, would have applied Krivokapic's to conventional stack layers or Fairbairn's etched layer to assure the proper degree of etching. *See KSR*, 550 U.S. at 418 (In making an obviousness determination one "can take account of the inferences and creative steps that a person of ordinary skill in the art would employ").

The Appellants argue that "*Krivokapic* merely teaches and suggests further etching of an under-etched workpiece if, and only if, the desired etch results were not obtained during a first etch" (Br. 5; Reply Br. 5).

That argument is not persuasive because regardless of whether, in some instances, the wafer is either conforming or is over-etched and discarded, the Appellants' multi-pass process claim requirement would be met when Krivokapic's re-etch process is applied to under-etched layers.

Conclusion of Law

The Appellants have not shown reversible error in the Examiner's determination that the applied references would have rendered prima facie

obvious, to one of ordinary skill in the art, a process comprising measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on a substrate, and executing a multi-pass process in which, while forming the at least one structure, the substrate is processed more than once by a measurement process, an etch process and at least one post-etch process.

DECISION/ORDER

The rejections under 35 U.S.C. § 103 of claims 1-18 and 36-53 over Fairbairn in view of Choo, Krivokapic and Perry, and claims 19-21 over Fairbairn in view of Choo, Krivokapic, Perry and Morgenstern are affirmed.

It is ordered that the Examiner's decision is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

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